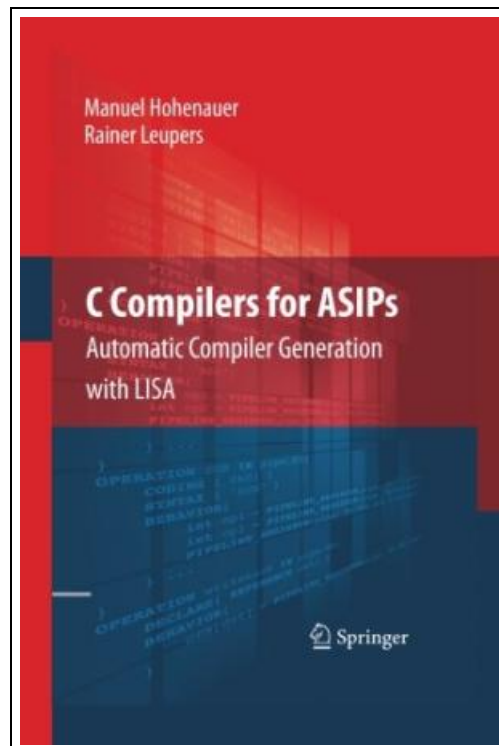


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1. Motivation Digital information technology has revolutionized the world during the last few decades. Today about 98% of programmable digital devices are actually embedded [132]. These embedded systems have become the main application area of information technology hardware and are the basis to deliver the sophisticated functionality of today's technical devices. As shown in Fig. 1. 1(a), current forecasts predict a worldwide embedded system market of \$88 billion in 2009. Millions of Gates 40 25 300 2004 35 Available Gates 2009 250 20 Used Gates AAGR 30 200 Design Productivity Gap 25 15 Design Productivity Gap 20 150 10 15 100 10 5 50 32 55 25 50 5 20 47 43 10 8 123 0,8 0 0 0 1993 1995 1997 1999 2001 2003 2005 America Europe Japan Asia-Pacific (a) Global embedded systems revenue and (b) Crisis of complexity [217] average annual growth rate (AAGR) [103] Fig. 1. 1 Embedded system design Over the past few years, the ever-increasing complexity and performance requirements of new wireless communications, automotive and consumer electronics applications are changing the way embedded systems are designed and implemented today. In conformity with Moore's law [99], one driving force is the rapid progress in deep-submicron process technologies. Chip designers and manufacturers have constantly pushed the envelope of technological and physical constraints. In fact, designers have more gates at their disposal than ever before. However, current M. Hohenauer, R. Leupers, C Compilers for ASIPs, 1 DOI 10.1007/978-1-4419-1176-6 1, C Springer Science+Business Media, LLC 2010 \$Billions 2 1 Introduction mainstream embedded system designs are not using at least 50% of the silicon area available to them (Fig. 1. 1(b)). The growth in design complexity threatens to outpace the designer's productivity, on account of unmanageable design sizes and the need for more design iterations due to deep-submicron effects. This phenomenon is also referred to as a crisis of complexity [103] and comes along with exponentially growing non-recurring engineering (NRE) costs (Fig. 1. 2) to design and manufacture chips. Understandably, these costs only amortize for very large volumes or high-end products. \$100. 000. 000. 000,00 \$10. 000. 000. 000,00 \$1. 000. 000. 000,00 \$100. 000. 000,00 RTL Methodology Future Improvements \$10. 000. 000,00 1990 1995 2000 2005 2010 2015 Fig. 1.



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