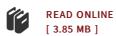# Embedded Multiprocessor System-On-Chip for Access Network Processing

By Mohamed Bamakhrama

GRIN Verlag. Paperback. Condition: New. 98 pages. Dimensions: 8.3in. x 5.8in. x 0.2in.Masters Thesis from the year 2007 in the subject Computer Science - Applied, grade: 1. 0, Technical University of Munich (Institute for Informatics), 82 entries in the bibliography, language: English, abstract: Multicore systems are dominating the processor market; they enable the increase in computing power of a single chip in proportion to the Moores law-driven increase in number of transistors. A similar evolution is observed in the system-on-chip (SoC) market through the emergence of multi-processor SoC (MPSoC) designs. Nevertheless, MPSoCs introduce some challenges to the system architects concerning the efficient design of memory hierarchies and system interconnects while maintaining the low power and cost constraints. In this master thesis, I try to address some of these challenges: namely, non-cache coherent DMA transfers in MPSoCs, low instruction cache utilization by OS codes, and factors governing the system throughput in MPSoC designs. These issues are investigated using the empirical and simulation approaches. Empirical studies are conducted on the Danube platform. Danube is a commercial MPSoC platform that is based on two 32-bit MIPS cores and developed by Infineon Technologies AG for deployment in access network processing equipments such as integrated...

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