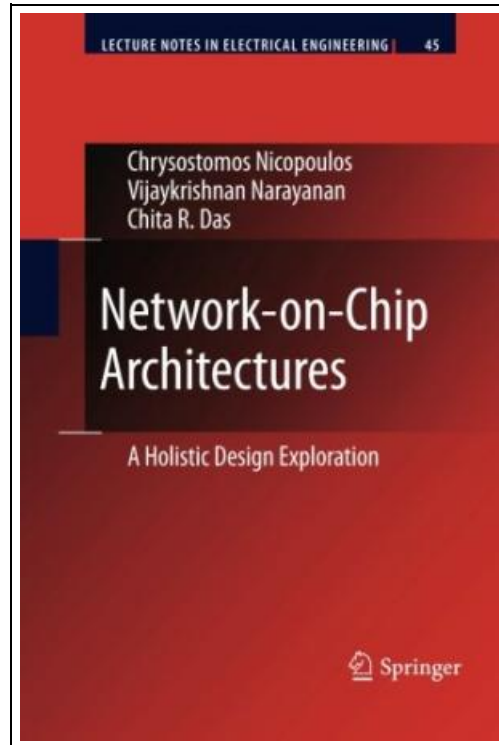


## Network-On-Chip Architectures: A Holistic Design Exploration



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## NETWORK-ON-CHIP ARCHITECTURES: A HOLISTIC DESIGN EXPLORATION



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Springer. Paperback. Book Condition: New. Paperback. 223 pages. Dimensions: 9.2in. x 6.1in. x 0.6in. The continuing reduction of feature sizes into the nanoscale regime has led to dramatic increases in transistor densities. Integration at these levels has highlighted the criticality of the on-chip interconnects. Network-on-Chip (NoC) architectures are viewed as a possible solution to burgeoning global wiring delays in many-core chips, and have recently crystallized into a significant research domain. On-chip networks instill a new flavor to communication research due to their inherently resource-constrained nature. Despite the lightweight character demanded of the NoC components, modern designs require ultra-low communication latencies in order to cope with inflating data bandwidths. The work presented in *Network-on-Chip Architectures* addresses these issues through a comprehensive exploration of the design space. The design aspects of the NoC are viewed through a pentafaceted prism encompassing five major issues: (1) performance, (2) silicon area consumption, (3) powerenergy efficiency, (4) reliability, and (5) variability. These five aspects serve as the fundamental design drivers and critical evaluation metrics in the quest for efficient NoC implementations. The research exploration employs a two-pronged approach: (a) MICRO-architectural innovations within the major NoC components, and (b) MACRO-architectural choices aiming to seamlessly merge the interconnection backbone with the remaining system modules. These two research threads and the aforementioned five key metrics mount a holistic and in-depth attack on most issues surrounding the design of NoCs in multi-core architectures. This item ships from multiple locations. Your book may arrive from Roseburg, OR, La Vergne, TN. Paperback.



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